REDUCTION OF BORON DIFFUSIVITY IN PFETS

ABSTRACT OF THE DISCLOSURE

A stressed film applied across a boundary defined by a structure or a body (e.g. substrate or layer) of semiconductor material provides a change from tensile to compressive stress in the semiconductor material proximate to the boundary and is used to modify boron diffusion rate during annealing and thus modify final boron concentrations. In the case of a field effect transistor, the gate structure may be formed with or without sidewalls to regulate the location of the boundary relative to source/drain, extension and/or halo implants. Different boron diffusion rates can be produced in the lateral and vertical directions and diffusion rates comparable to arsenic can be achieved. Reduction of junction capacitance of both nFETs and pFETs can be achieved simultaneously with the same process steps.